Short Papers

Ka-Band High Efficiency Power Amplifier MMIC with 0.30 μm MESFET for High Volume Applications

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***Abstract*—A single-ended three-stage MESFET power amplifier designed for high-volume, low-cost applications shows an average of 15–21% power added efficiency in *Ka*-band with 100–150 mW of power output over 30–35 GHz. $\Delta < S21$ with power saturation, an important parameter in phased array applications, is also reported. Efficiencies as high as 28% are measured on good wafers with high on-wafer repeatability under power drive.**

I. Introduction

Power amplifiers with MESFET have been reported in *Ka*-band [1]–[2] for high-efficiency, high-power applications. These amplifiers use 0.25–3 μm gate MBE MESFET with very high transconductance (~300 ms/mm) [1], fabricated on heavily doped material (8×10^{17} cm^{-3}). Even though the power performance of the balanced amplifier reported [2] is good, no information is given on its efficiency and how it varies over frequency. In this article we report the performance of a three-stage power amplifier designed with devices having lower channel doping ($3\text{–}4 \times 10^{17}$ cm^{-3}) and lower transconductance. The discrete device has an MSG of 6–7 dB at 35 GHz. The average f_t for a 200 μm device at VDS = 5 and Ids = 50% Idss is 27 GHz. The f_{max} of the device is estimated by extrapolation of the equivalent circuit model and is found to lie between 80–90 GHz for the same bias point. The design was also made broadband enough to improve the yield and manufacturability. Even though a survey article [3] discusses the millimeter-wave power amplifications using discrete HEMT devices, not much published data is available on power HEMT-MMIC in millimeter-wave to compare the efficiencies.

II. Fabrication

The power amplifiers were fabricated on MBE material with a 1900 Å thick channel layer doped to a level of 3.2 e17 cm^{-3} and a capping layer doped to 6.4 e17 cm^{-3}. A lower channel doping accounts for the lower transconductance compared to results in [1]. Peak dc g_m for our devices ranged from 170–200 mS/mm and dc g_m at 1/2 Idss with a 2V drain bias was 150 mS/mm. Typical channel current at Idss was 350 mA/mm. The lower channel and ledge doping in devices reduces the etch time sensitivity of the ledge and gate recess etch steps and leads to improved manufacturability. In spite of the reduced channel doping, power-added efficiency as high as 28% was achieved. The *Ka*-band gain of the devices was found to be significantly influenced by gate resistance and 0.3 μm gate devices had higher gain at 35 GHz than 0.25 μm gate devices.

The transmitter MMIC is fabricated using an *e*-beam/stepper lithography process. All lithography except the ledge and gate recess steps are done on an optical stepper for high wafer throughput. The critical gate and ledge levels are done by direct write *e*-beam lithography. Device isolation is achieved by proton implantation with a photoresist mask covering the device active area. The 0.3 μm gate in the devices is placed in the center of a 1 μm wide ledge recess etched through the capping layer. Frontside processing steps such as ohmic contact and silicon nitride capacitor formation use conventional GaAs MESFET processing techniques. Backside processing of the wafers includes thinning to 4 mil, reactive ion etching of via holes, backside gold plating, and etching streets in the gold plating for chip separation.

III. Design and Results

The three stages of the amplifier employ devices with 0.3×100 μm^2 (four fingers), 0.3×200 μm^2 (eight fingers), and 0.3×400 μm^2 (10 fingers) gate periphery. The amplifier has been designed to operate in class AB mode. All three stages have one common drain supply and one common gate supply. Even though a common bus is involved for the bias supply, individual stages are ac decoupled with bias cap and resistors; coils (RF chokes) are included in the supply line to filter out any residual ripple on the dc line. This biasing arrangement makes the amplifier extremely insensitive with respect to outside bias connections. The amplifier has also shown very stable operation over wide bias variation (VDS = 2–6V, Ids = 0% to 100% Idss). The amplifier was simulated using commercial software LIBRA-2.1 and Curtice large signal model (MODEL = 2, in LIBRA). A similar type of large signal model (MODEL = 2) has been reported [4]. The simulation predicted an output power of 140 mW at 35 GHz with 15% power added efficiency with a drive level of 10 dBm. Each stage output is matched to a large signal load (the real part of which is determined by *I-V* characteristics and the imaginary part by small signal total output capacitance). Fig. 1 shows the layout of the three-stage amplifier. It measures 1.42 mm × 2.52 mm on 0.1 mm GaAs. The dc characteristics of a 200 μm FET is shown in Fig. 2. The amplifier was operated at VDS = 5V with VGS = −1.4V (40–50% Idss). Fig. 3 shows the frequency response of the amplifier with a nominal P_{in} ~ 10–11 dBm. Fig. 4 shows the saturation characteristics at 33, 34, and 35 GHz. Also included in the figures is the differential transmission phase ($\Delta < S21$) as the amplifier saturates. $\Delta < S21$ is given with the value of $< S21$ at $P_{in} = 0$ dBm taken as reference. The device itself can deliver 350–400 mw/mm over 31–35 GHz. This is calculated after taking into account the output circuit loss of approximately −.7 dB. The output circuit loss (power gain) is calculated by using a capacitor "*Q*" of 16 at 35 GHz and transmission line loss equal to 1.25 times the bulk gold resistivity. A capacitor "*Q*" of 22 was measured in *X*-band (10 GHz).

At 3 dB compression points, (with respect to Pout, $P_{in} = 0$ dBm) $\Delta < S21$ measures −19° at 33 GHz, −18° at 34 GHz and −17°

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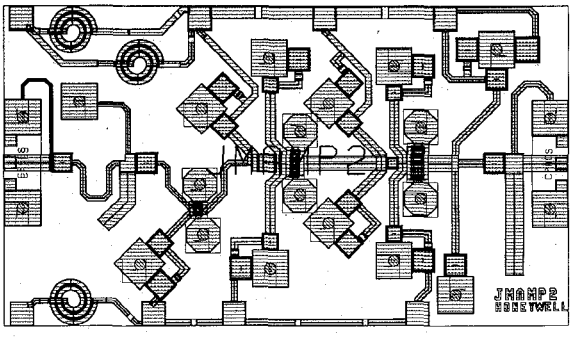


Fig. 1. Layout of a three-stage power amplifier. The chip measures 2.52 × 1.42 × 0.10 mm³.

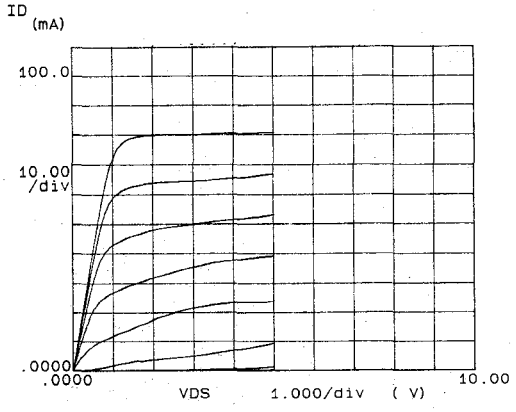


Fig. 2. DC characteristics of a 200 μm MESFET used in the amplifier. Idss ~350–400 mA/mm, gm (intrinsic) ~150 ms/mm at 50% Idss and VDS = 5 V.

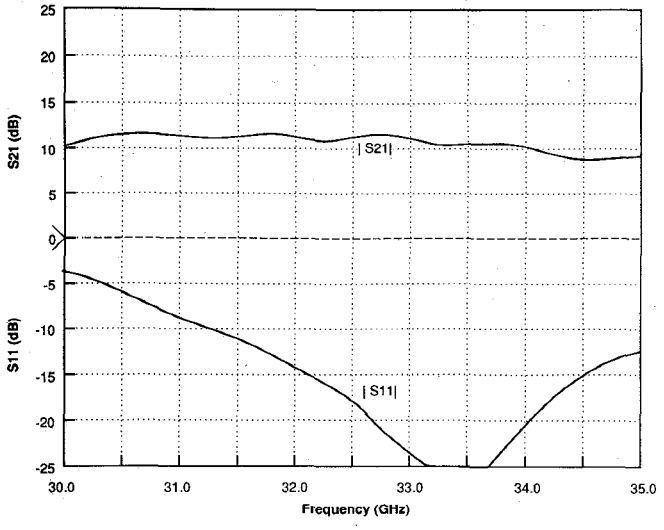
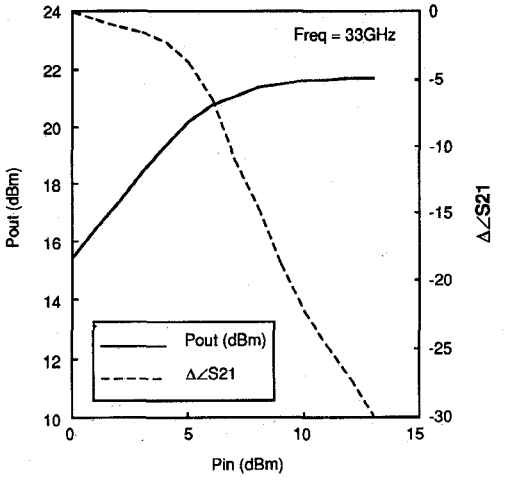
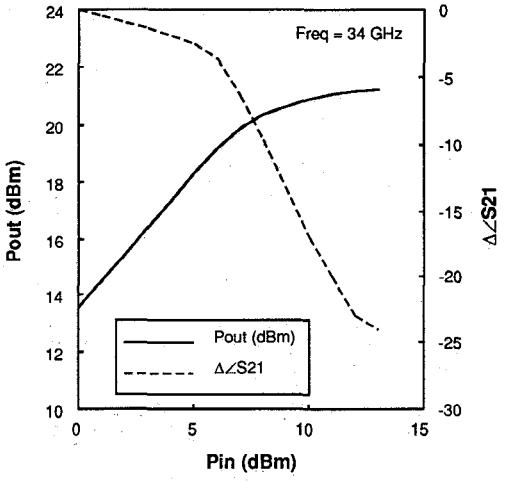


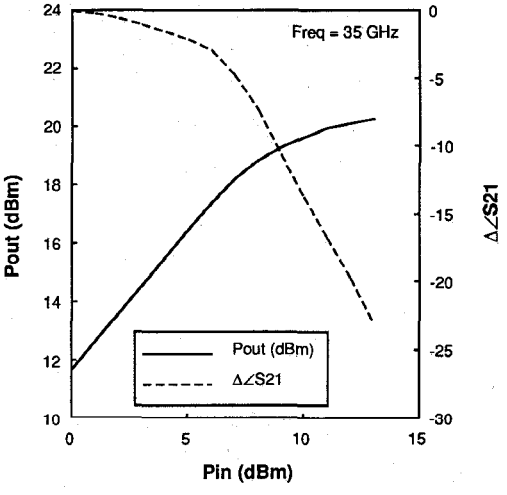
Fig. 3. Amplifier frequency response with nominal 10–11 dBm of input (wafer #1).



(a)



(b)



(c)

Fig. 4. Power saturation characteristics of the amplifier. Both Pout (dBm) and Δ $<S21$ are plotted with input drive. When all stages go uniformly into saturation, the deviation in $<S21$ should gradually fall for each extra dB into saturation. (a) 33 GHz, (b) 34 GHz, (c) 35 GHz.

at 35 GHz. From 2–3 dB compression point, the changes in transmission phase are −4° at 31 GHz, −3.5° at 34 GHz and −3° at 35 GHz. The deviation in $<S21$ is much less when the amplifier is in saturation. This is to be expected, and it also shows that all the stages in the amplifier are getting uniformly into saturation. In phased array applications the nature of variation of $<S21$ with power is important information for minimizing the phase error in each element. Fig. 5 shows the power-added efficiency and the corresponding drain current over the frequency, 30–35 GHz with the output power compressed nearly by 3 dB. Also shown in the same figure are the maximum efficiency values that occur at nearly 4 dB compression point. Even though the gain falls by 1 dB, the increase in drain current gradually flattens out, which leads to slightly higher efficiency at higher power compression.

In Fig. 6 we show the performance of the same design on a wafer

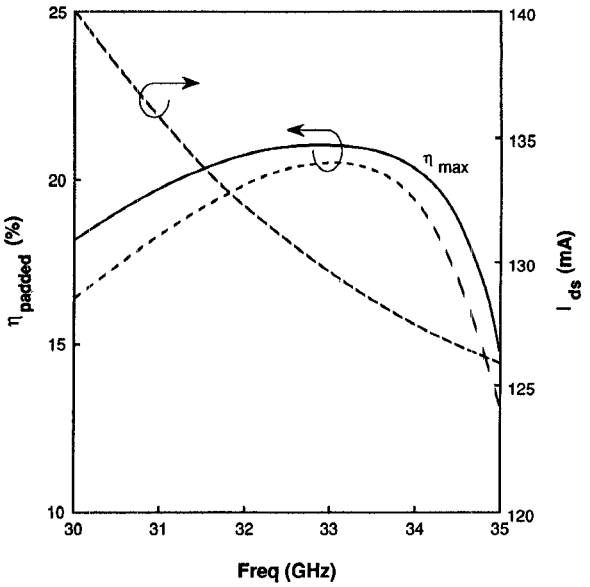


Fig. 5. Power-added efficiency and the corresponding drain current at that efficiency over frequency. Output power is approximately 3 dB compressed. Also shown are the maximum power-added efficiencies achieved at a higher compression point (nearly 1 dB more). This increase in efficiency is mainly due to less increase in drain current. Ids at P_{in} = 0 dBm is 120 mA. VDS = 5V. VGS = −1.4V.

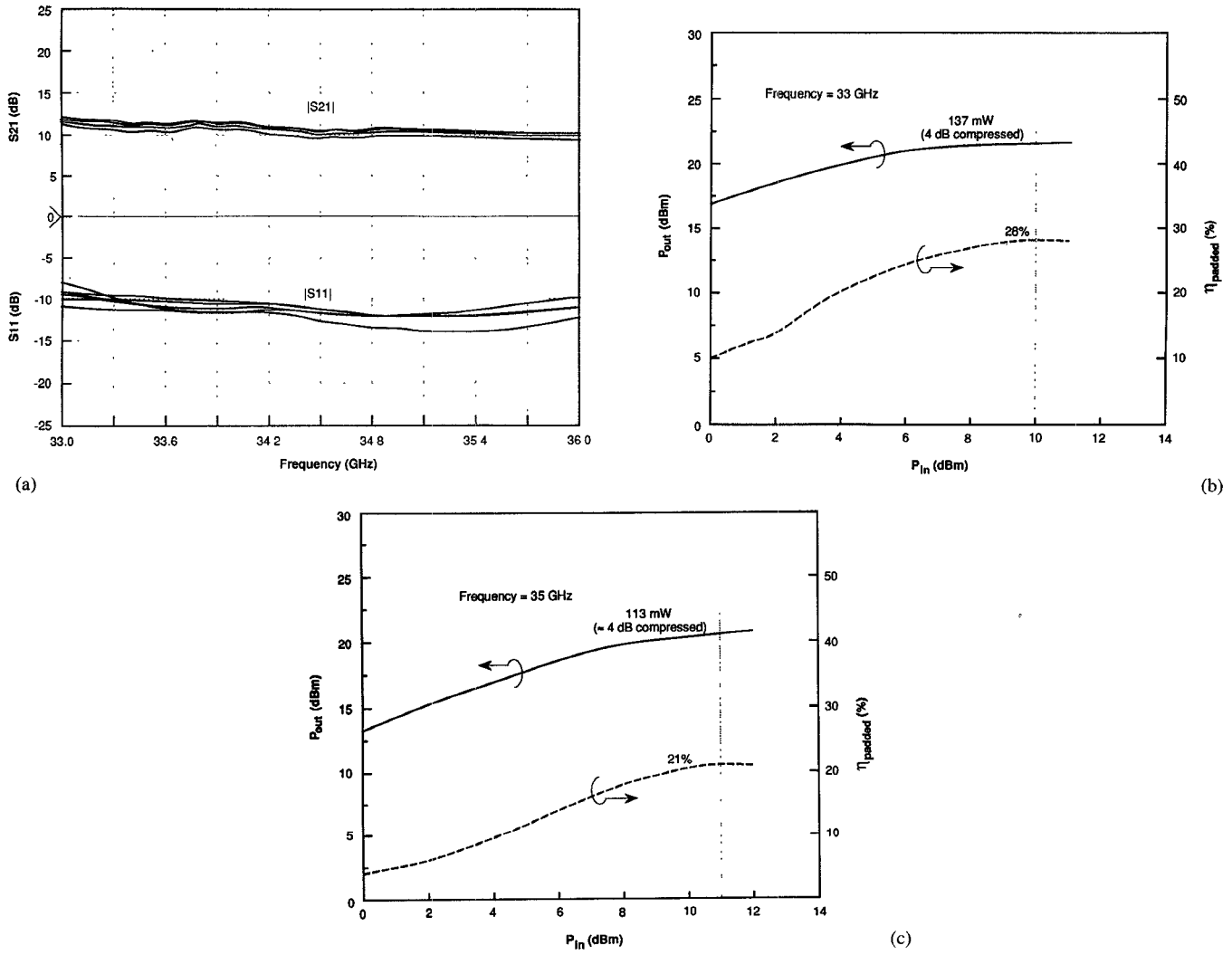


Fig. 6. (a) Performance of five amplifiers from the same wafer (wafer #8) giving good results over the band of interest (33–36 GHz). (b) Power saturation characteristics at 33 GHz. (c) Power saturation characteristics at 35 GHz.

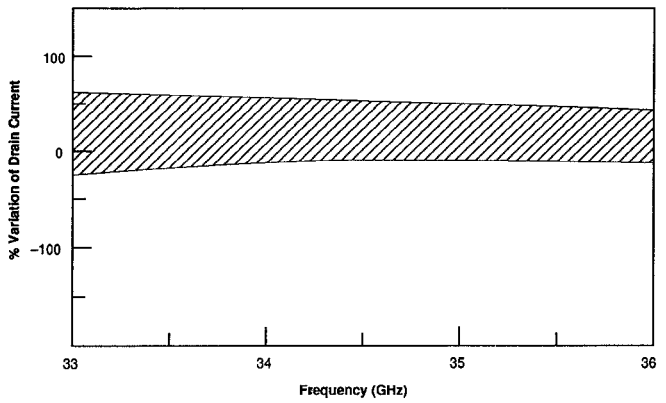


Fig. 7. Bias sensitivity of the amplifier at VDS = 5V. The drain current is varied to change the gain by ±0.5 dB (max) from the maximum efficiency point. The drain current is changed with gate voltage. The maximum efficiency occurs with $P_{in} \sim 10$ dBm; so the input is maintained at 10 dBm. The amplifier can be maintained well under saturation with more than 50% variation in drain current over the frequency range 33–36 GHz.

with the highest efficiency. The response is shown in Fig. 6(a) for five amplifiers with the same drain and gate voltages (VDS = 5V VGS = −1.35V) over a narrower band 33–36 GHz, the nominal input is 10–11 dBm (exactly 10 dBm at 34.5 GHz). The five amplifiers are chosen from five reticles at random approximately from the center of the wafer. The response shows the repeatability of the design at least from the same wafer over the band of interest. Fig. 6(b) and (c) show the power saturation characteristics at 33 GHz and 35 GHz, respectively. The efficiency reaches as high as 28% at 33 GHz and 21% at 35 GHz at a high compression level (3–4 dB). At those efficiencies, the power outputs are 137 mW at 33 GHz and 113 mW at 35 GHz, and the drain currents are 91 mA at 33 GHz and 95 mA at 35 GHz and corresponding P_{in}'s are 10 dBm at 33 GHz and 11 dBm at 35 GHz. Finally Fig. 7 shows the bias sensitivity of the amplifiers. The drain bias is fixed at VDS = 5V and gate bias varied to make the gain change by ±0.5 dB at the maximum efficiency bias point. At higher drain current, the gain first increases before it starts dropping; the efficiency also degrades with the gain variation. All the results reported here are taken with RF probes with the chip placed on a metal block without being soldered. The yield window, being application specific, was set at G ±2 dB, where G is the gain with nominal 10 dBm input. G in our case was set at 10 dB over 33–35 GHz. The results reported here are from a nominal wafer and also the best wafer that we measured.

IV. Conclusion

A broad *Ka*-band three-stage power MMIC is successfully demonstrated which is designed with MBE MESFET devices with moderate doping levels and device transconductance. The design is quite tolerant to process and bias variations. The performance is suitable for the applications requiring high volume, low cost and manufacturable process. The amplifier shows fairly high efficiency over a broadband, which is more than adequate in smart ammunition applications.

Acknowledgment

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Criteria for the Onset of Oscillation In Microwave Circuits

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***Abstract*—A commonly used criterion for oscillator startup is demonstrated not to be universally valid. In order to investigate startup conditions, the Nyquist stability criterion is written in terms of microwave quantities. It is shown that widely available microwave CAD can be used to create Nyquist stability plots. Since the Nyquist criterion gives only global stability information, a convenient graphical criterion is developed to determine whether an oscillation will start up near a particular resonance frequency.**

I. Introduction

Many texts and papers use the following criteria for oscillation start up at resonance,

$$|\Gamma_d||\Gamma_c| > 1 \quad \text{and} \quad \phi_d + \phi_c = 0 \tag{1}$$

where Γ_d is the reflection coefficient seen looking into an active device, Γ_c is the reflection coefficient seen looking into a passive resonating circuit, and ϕ_d, ϕ_c are the angles associated with each reflection coefficient. The resonance frequency is defined to be the frequency at which ϕ_d and ϕ_c sum to zero.

This condition is intuitively attractive, but it does not accurately predict instability or stability in all cases. For example, consider the two circuits in Fig. 1. These simple circuits are easily analyzed by conventional circuit theory techniques. Circuit A has left half plane poles and thus is stable. Circuit B has right half plane poles and is unstable. The reflection coefficients Γ_d and Γ_c are 6 and 0.091, respectively at resonance (50 Ω reference). Criteria (1) predict that both circuits will be stable. This is clearly the wrong conclusion for circuit B.

In this paper, we write the well-known Nyquist stability criterion in terms of quantities which are commonly used in microwave active circuit design. In Section I, it will be shown that the Nyquist plot for microwave circuits can be easily generated using commercially available microwave CAD.

Although the Nyquist criterion rigorously determines the stability of a circuit, it does not give any information about oscillation frequencies. It just answers the question, "Is it stable or not?" In Section II, we consider the case where a circuit is assumed to be

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